International **IR** Rectifier

AUTOMOTIVE MOSFET

IRFBA1404PPbF

HEXFET® Power MOSFET

Typical Applications
- Anti-lock Braking Systems (ABS)
- Electric Power Steering (EPS)
- Electric Braking
- Radiator Fan Control
- Lead-Free

Benefits
- Advanced Process Technology
- Ultra Low On-Resistance
- Increase Current Handling Capability
- 175°C Operating Temperature
- Fast Switching
- Dynamic dv/dt Rating
- Repetitive Avalanche Allowed up to Tjmax
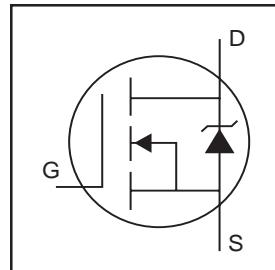
$V_{DSS} = 40V$

$R_{DS(on)} = 3.7m\Omega$

$I_D = 206A$⑥

Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this MOSFET are a 175°C junction operating temperature, fast switching speed and improved ruggedness in single and repetitive avalanche. The Super-220 ™ is a package that has been designed to have the same mechanical outline and pinout as the industry standard TO-220 but can house a considerably larger silicon die. The result is significantly increased current handling capability over both the TO-220 and the much larger TO-247 package. The combination of extremely low on-resistance silicon and the Super-220 ™ package makes it ideal to reduce the component count in multiparalled TO-220 applications, reduce system power dissipation, upgrade existing designs or have TO-247 performance in a TO-220 outline. This package has been designed to meet automotive, Q101, qualification standard.

These benefits make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

Super-220™

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	206⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	145⑥	
I_{DM}	Pulsed Drain Current ①	650	
P_D @T_C = 25°C	Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	480	mJ
I_{AR}	Avalanche Current①	See Fig.12a, 12b, 14, 15	A
E_{AR}	Repetitive Avalanche Energy①		mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-40 to + 175	°C
T_{STG}	Storage Temperature Range	-55 to + 175	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Recommended clip force	20	N

Electrical Characteristics @ T$_J$ = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V$_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	——	——	V	V$_{GS}$ = 0V, I$_D$ = 250µA
ΔV$_{(BR)DSS}$/ΔT$_J$	Breakdown Voltage Temp. Coefficient	——	0.036	——	V/°C	Reference to 25°C, I$_D$ = 1mA
R$_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	3.7	mΩ	V$_{GS}$ = 10V, I$_D$ = 95A ④
V$_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V$_{DS}$ = 10V, I$_D$ = 250µA
g$_{fs}$	Forward Transconductance	106	——	——	S	V$_{DS}$ = 25V, I$_D$ = 60A
I$_{DSS}$	Drain-to-Source Leakage Current	——	——	20	µA	V$_{DS}$ = 40V, V$_{GS}$ = 0V
		——	——	250		V$_{DS}$ = 32V, V$_{GS}$ = 0V, T$_J$ = 150°C
I$_{GSS}$	Gate-to-Source Forward Leakage	——	——	200	nA	V$_{GS}$ = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V$_{GS}$ = -20V
Q$_g$	Total Gate Charge	——	160	200		I$_D$ = 95A
Q$_{gs}$	Gate-to-Source Charge	——	35	——	nC	V$_{DS}$ = 32V
Q$_{gd}$	Gate-to-Drain ("Miller") Charge	——	42	60		V$_{GS}$ = 10V
t$_{d(on)}$	Turn-On Delay Time	——	17	——		V$_{DD}$ = 20V
t$_r$	Rise Time	——	140	——	ns	I$_D$ = 95A
t$_{d(off)}$	Turn-Off Delay Time	——	72	——		R$_G$ = 2.5Ω
t$_f$	Fall Time	——	26	——		R$_D$ = 0.21Ω ④
L$_D$	Internal Drain Inductance	——	2.0	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L$_S$	Internal Source Inductance	——	5.0	——		
C$_{iss}$	Input Capacitance	——	7360	——		V$_{GS}$ = 0V
C$_{oss}$	Output Capacitance	——	1680	——		V$_{DS}$ = 25V
C$_{rss}$	Reverse Transfer Capacitance	——	240	——	pF	ƒ = 1.0MHz, See Fig. 5
C$_{oss}$	Output Capacitance	——	6630	——		V$_{GS}$ = 0V, V$_{DS}$ = 1.0V, ƒ = 1.0MHz
C$_{oss}$	Output Capacitance	——	1490	——		V$_{GS}$ = 0V, V$_{DS}$ = 32V, ƒ = 1.0MHz
C$_{oss}$ eff.	Effective Output Capacitance ⑤	——	1540	——		V$_{GS}$ = 0V, V$_{DS}$ = 0V to 32V
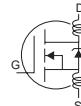
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I$_S$	Continuous Source Current (Body Diode)	——	——	206⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I$_{SM}$	Pulsed Source Current (Body Diode) ①	——	——	650		
V$_{SD}$	Diode Forward Voltage	——	——	1.3	V	T$_J$ = 25°C, I$_S$ = 95A, V$_{GS}$ = 0V ④
t$_{rr}$	Reverse Recovery Time	——	71	110	ns	T$_J$ = 25°C, I$_F$ = 95A
Q$_{rr}$	Reverse Recovery Charge	——	180	270	nC	di/dt = 100A/µs ④
t$_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L$_S$+L$_D$)				
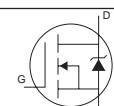
Thermal Resistance

	Parameter	Typ.	Max.	Units
R$_{θJC}$	Junction-to-Case	——	0.50	
R$_{θCS}$	Case-to-Sink, Flat, Greased Surface	0.5	——	°C/W
R$_{θJA}$	Junction-to-Ambient	——	58	

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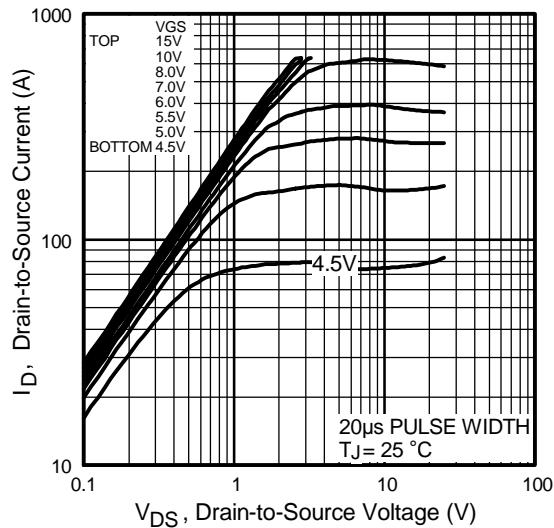
Fig 1. Typical Output Characteristics

Graph: I_D, Drain-to-Source Current (A) vs V_{DS}, Drain-to-Source Voltage (V)
VGS TOP 15V, 10V, 8.0V, 7.0V, 6.0V, 5.5V, 5.0V, BOTTOM 4.5V
4.5V
20µs PULSE WIDTH
$T_J = 25\,^{\circ}C$

Fig 2. Typical Output Characteristics

Graph: I_D, Drain-to-Source Current (A) vs V_{DS}, Drain-to-Source Voltage (V)
VGS TOP 15V, 10V, 8.0V, 7.0V, 6.0V, 5.5V, 5.0V, BOTTOM 4.5V
4.5V
20µs PULSE WIDTH
$T_J = 175\,^{\circ}C$
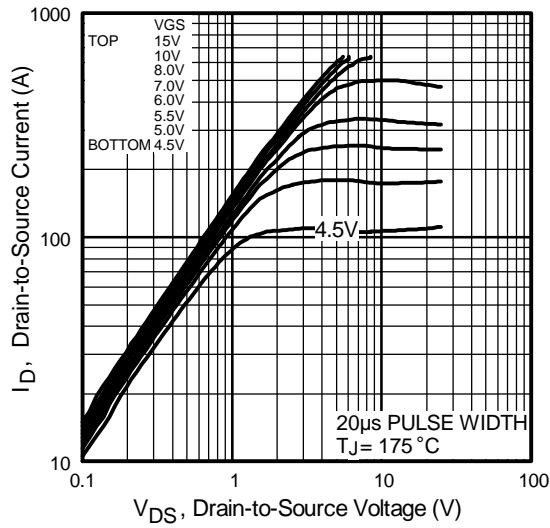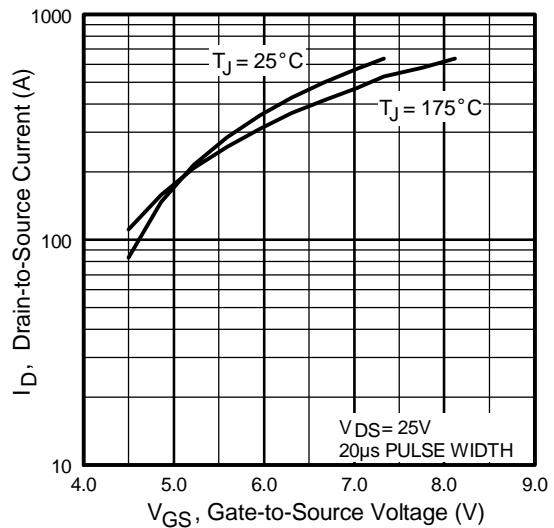
Fig 3. Typical Transfer Characteristics

Graph: I_D, Drain-to-Source Current (A) vs V_{GS}, Gate-to-Source Voltage (V)
$T_J = 25\,^{\circ}C$
$T_J = 175\,^{\circ}C$
$V_{DS} = 25V$
20µs PULSE WIDTH
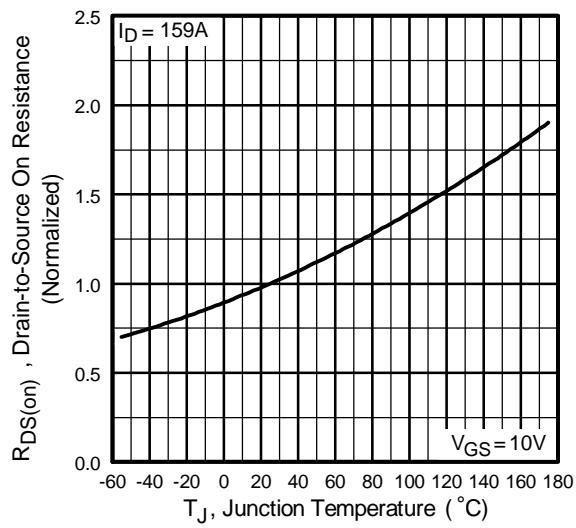
Fig 4. Normalized On-Resistance Vs. Temperature

Graph: $R_{DS(on)}$, Drain-to-Source On Resistance (Normalized) vs T_J, Junction Temperature ($^{\circ}C$)
$I_D = 159A$
$V_{GS} = 10V$

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$V_{GS} = 0V$,   f = 1MHz
$C_{iss} = C_{gs} + C_{gd}$, C_{ds} SHORTED
$C_{rss} = C_{gd}$
$C_{oss} = C_{ds} + C_{gd}$
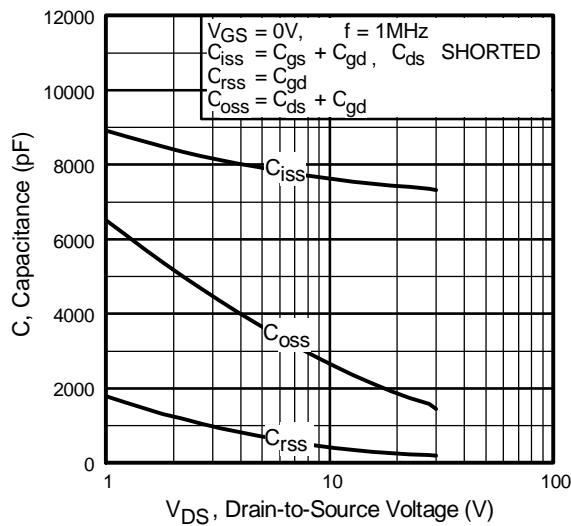
Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage
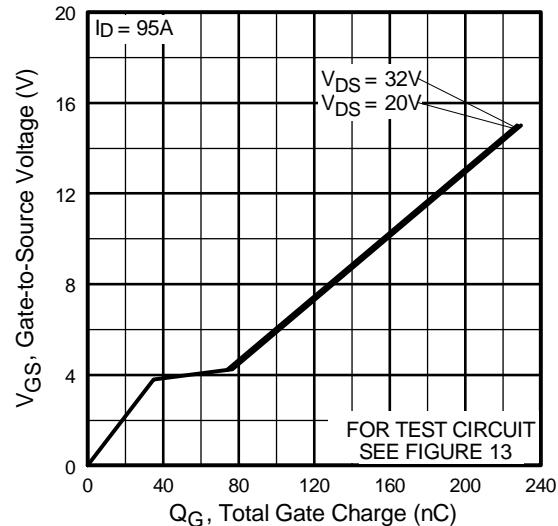
Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage
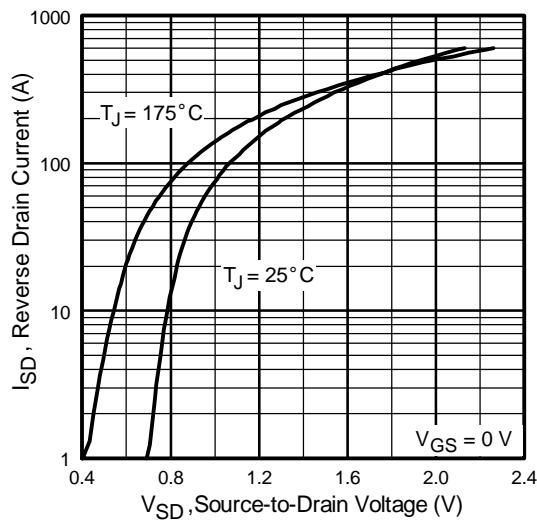
Fig 7. Typical Source-Drain Diode Forward Voltage
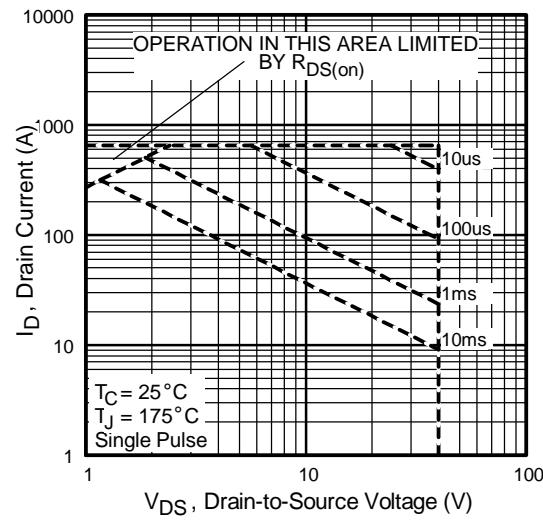

Fig 8. Maximum Safe Operating Area

4
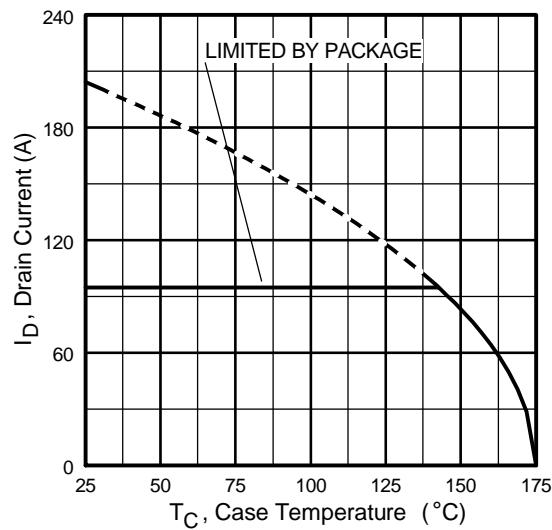
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Fig 9. Maximum Drain Current Vs.
Case Temperature
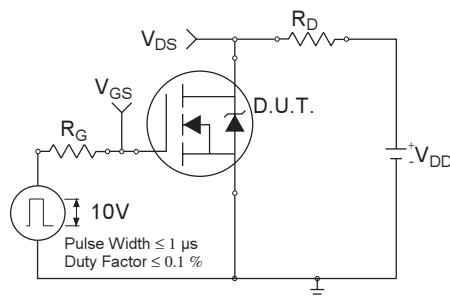
Fig 10a. Switching Time Test Circuit

V_{DS}
90%

10%
V_{GS}

$t_{d(on)}$ t_r $t_{d(off)}$ t_f
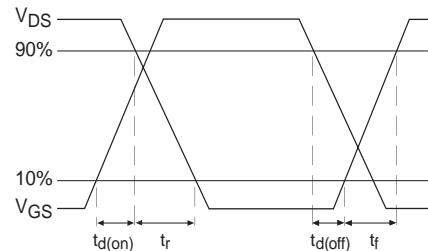
Fig 10b. Switching Time Waveforms

Notes:
1. Duty factor D = t_1 / t_2
2. Peak T_J = P_{DM} x Z_{thJC} + T_C
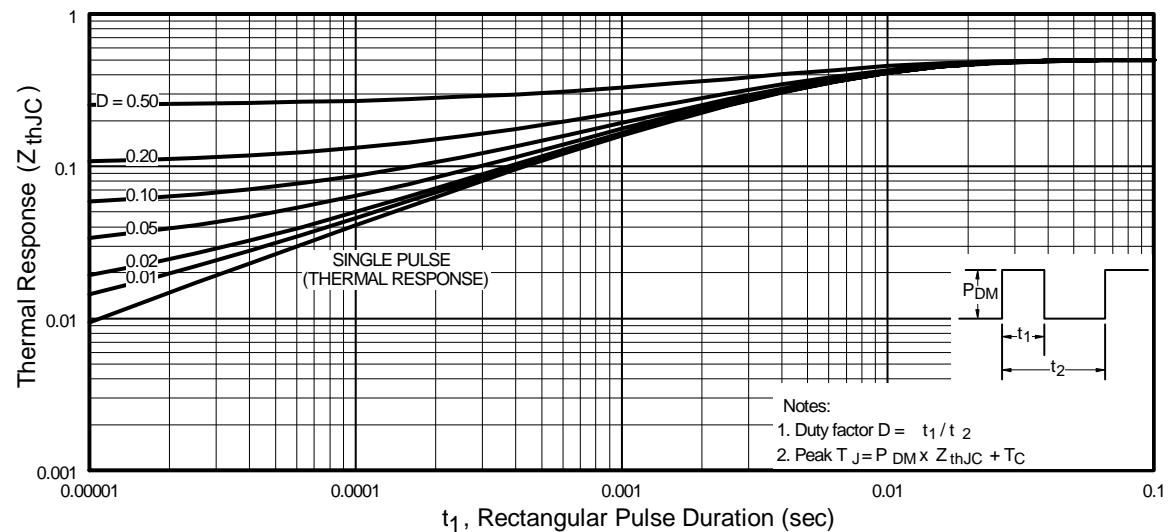
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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Fig 12a. Unclamped Inductive Test Circuit
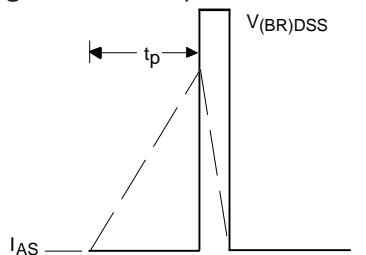

**Fig 12b.** Unclamped Inductive Waveforms
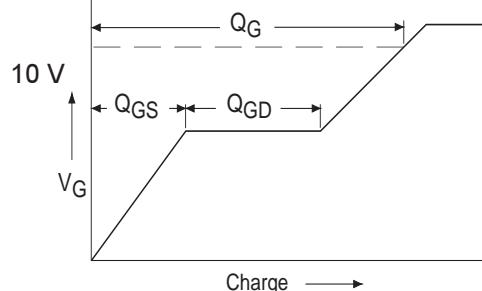
Fig 13a. Basic Gate Charge Waveform
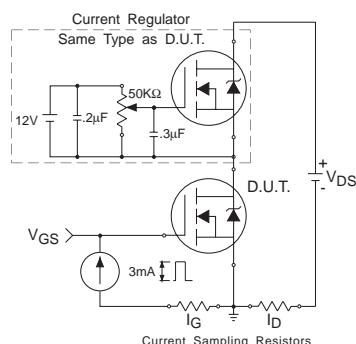
**Fig 13b.** Gate Charge Test Circuit
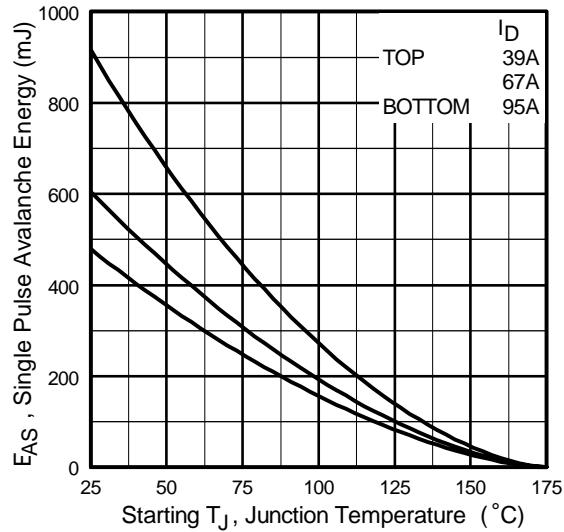

Fig 12c. Maximum Avalanche Energy
Vs. Drain Current
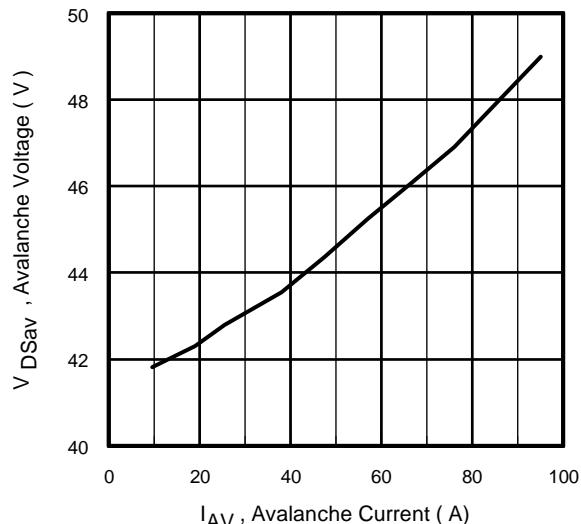
**Fig 12d.** Typical Drain-to-Source Voltage
Vs. Avalanche Current

6   www.irf.com

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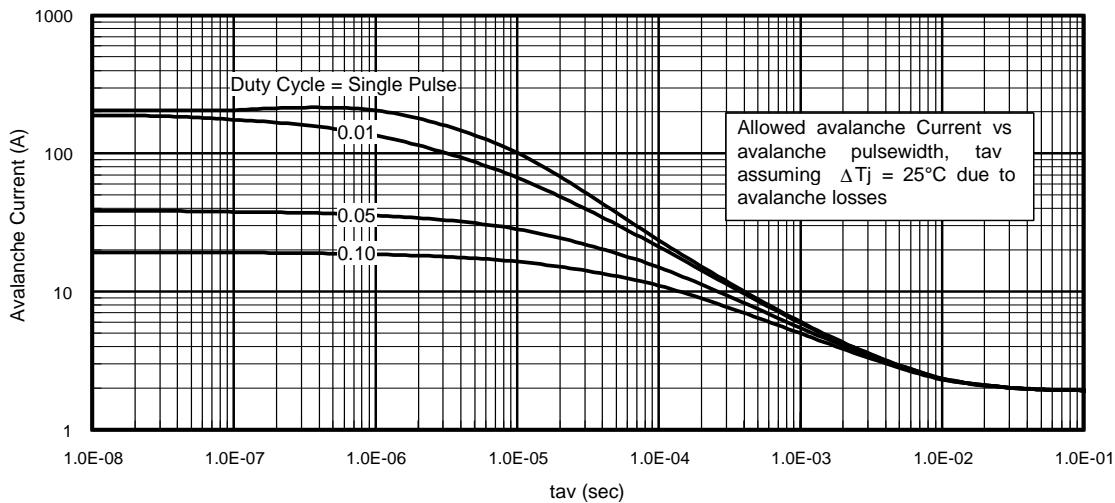
Fig 14. Typical Avalanche Current Vs.Pulsewidth

(Within Fig 14: Duty Cycle = Single Pulse; 0.01; 0.05; 0.10; Allowed avalanche Current vs avalanche pulsewidth, tav assuming $\Delta Tj = 25°C$ due to avalanche losses)

(Within Fig 15: TOP — Single Pulse; BOTTOM — 10% Duty Cycle; $I_D = 95A$)
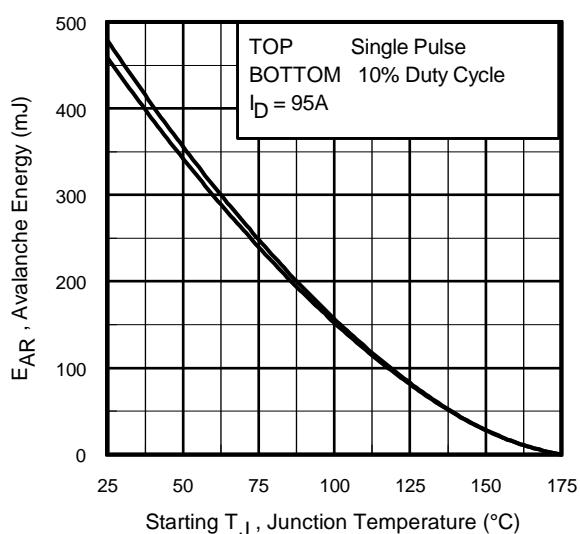
Fig 15. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
**(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\,(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\,(ave)} = 1/2\,(\,1.3 \cdot BV \cdot I_{av}) = \Delta T/\,Z_{thJC}$$
$$I_{av} = 2\Delta T/\,[1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\,(AR)} = P_{D\,(ave)} \cdot t_{av}$$

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Peak Diode Recovery dv/dt Test Circuit

D.U.T

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance
  Current Transformer

③

②

④

- dv/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

R_G

V_{DD}

① Driver Gate Drive

$D = \dfrac{P.W.}{Period}$

Period

P.W.

V_{GS}=10V *

② D.U.T. I_{SD} Waveform

Reverse
Recovery
Current

Body Diode Forward
Current

di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery
dv/dt

V_{DD}

Re-Applied
Voltage

Body Diode Forward Drop

④ Inductor Curent

Ripple ≤ 5%

I_{SD}

* V_{GS} = 5V for Logic Level Devices

Fig 16. For N-Channel HEXFET® Power MOSFETs

Super-220™ (TO-273AA) Package Outline
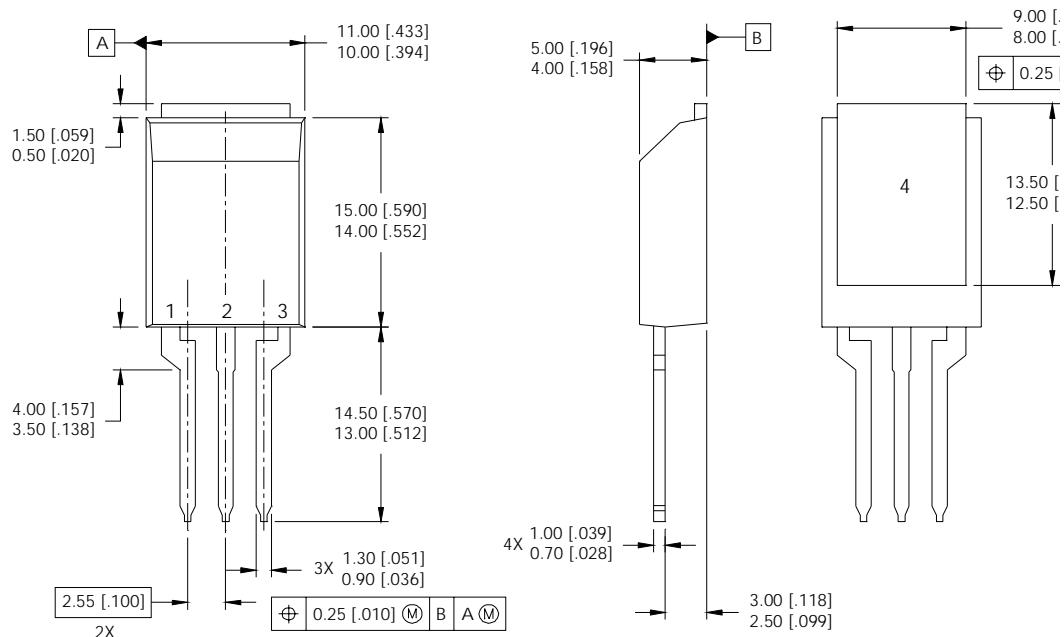
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-273AA.

LEAD ASSIGNMENTS

MOSFET	**IGBT**
1 – GATE	1 – GATE
2 – DRAIN	2 – COLLECTOR
3 – SOURCE	3 – EMITTER
4 – DRAIN	4 – COLLECTOR

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 0.11mH
   R_G = 25Ω, I_{AS} = 95A.

③ I_{SD} ≤ 95A, di/dt ≤ 150A/µs, V_{DD} ≤ $V_{(BR)DSS}$,
   T_J ≤ 175°C

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} . Refer to AN-1001

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 95A.

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Super-220 (TO-273AA) Part Marking Information

EXAMPLE: THIS IS AN IRFBA22N50A WITH
ASSEMBLY LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

PART NUMBER

INTERNATIONAL RECTIFIER
LOGO

IRFBA22N50A

IΩR   719C

17   89

DATE CODE
YEAR 7 = 1997

WEEK 19
LINE C

ASSEMBLY LOT CODE

TOP
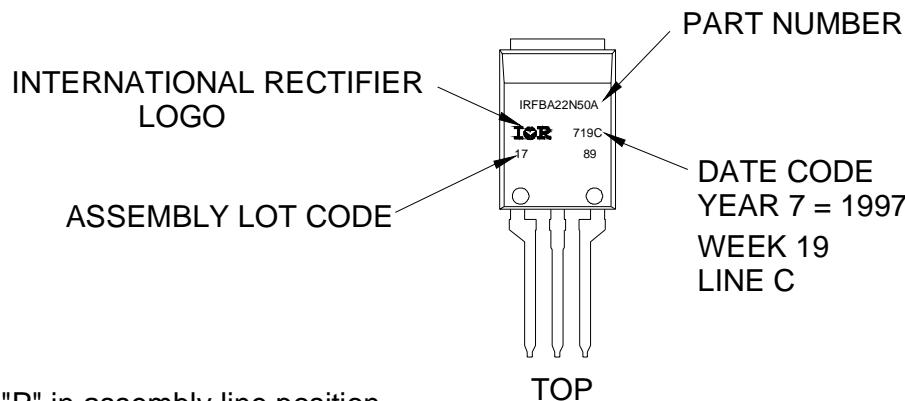
Note: "P" in assembly line position
indicates "Lead-Free"

Super-220™ not recommended for surface mount application

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.